### (19) World Intellectual Property Organization

International Bureau



# 

(43) International Publication Date 7 July 2005 (07.07.2005)

**PCT** 

# (10) International Publication Number WO 2005/062354 A1

(51) International Patent Classification<sup>7</sup>: H01L 21/265, 21/20, 21/336, 29/78

(21) International Application Number:

PCT/IB2004/052644

(22) International Filing Date: 2 December 2004 (02.12.2004)

(25) Filing Language:

English

(26) Publication Language:

**English** 

(30) Priority Data: 03104781.4 18 December 2003 (18.12.2003) EP

(71) Applicant (for all designated States except US): KONIN-KLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

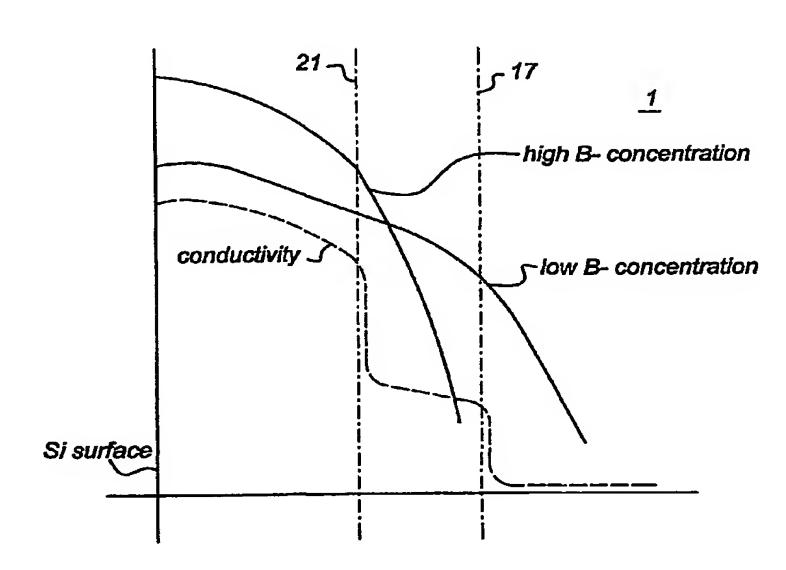
(75) Inventors/Applicants (for US only): PAWLAK, Bartlomiej, J. [PL/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DUFFY, Raymond, J. [IE/BE]; c/o Prof.

Holstlaan 6, NL-5656 AA Eindhoven (NL). LINDSAY, Richard [GB/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

- (74) Agents: ELEVELD, Koop, J. et al.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,

[Continued on next page]

(54) Title: A SEMICONDUCTOR SUBSTRATE WITH SOLID PHASE EPITAXIAL REGROWTH WITH REDUCED JUNCTION LEAKAGE AND METHOD OF PRODUCING SAME



(57) Abstract: Method of producing a semiconductor device, comprising: a) providing a semiconductor substrate, b) making a first amorphous layer in a top layer of the semiconductor substrate by a suitable implant, the first amorphous layer having a first depth, c) implanting a first dopant into the semiconductor substrate to provide the first amorphous layer with a first doping profile, d) applying a first solid phase epitaxial regrowth action to partially regrow the first amorphous layer and form a second amorphous layer having a second depth that is less than the first depth and activate the first dopant, e) implanting a second dopant into the semiconductor substrate to provide the second amorphous layer with a second doping profile with a higher doping concentration than the first doping profile, f)applying a second solid phase epitaxial regrowth action to regrow the second amorphous layer and activate the second dopant.



062354

## WO 2005/062354 A1



SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

#### Published:

— with international search report